AMENDMENTS TO THE DRAWINGS:

The attached drawing is a Replacement Sheet for Fig. 8. In box S1 of Fig. 8, the word "CONTEST" is replaced with the word --CONTEXT--. Replacement of the original sheet containing Fig. 8 is respectfully requested.

REMARKS

In the February 8, 2006 Office Action, claims 1-5, 7-13 and 15-19 were rejected under 35 USC § 102 as anticipated by U.S. Patent No. 6,216,193 to Lai.

In accordance with the foregoing, the specification, drawings and claims have been amended. Claims 1 and 9 have been canceled, claims 2, 4, 5, 7, 8, 10, 12, 13 and 15-17 have been amended and claims 20-22 have been added. Thus, claims 2-5, 7, 8, 10-13 and 15-22 are pending and under consideration. The rejections are traversed below.

Examiner Interview

The Applicant thanks the Examiner for granting an Interview conducted on June 15, 2006. During the Interview, the Examiner questioned support in the specification for the limitation "an instruction that is not a cause of said interrupt" as recited in claim 1. The Examiner required the claims clearly recite the continuation of an instruction without reloading lost data and the Examiner required clarification in the claim language whether first and second instructions were continued. The claims have been amended to clarify the claim language, based on the Examiner Interview.

Rejections under 35 USC 102

In item 2 on pages 2-6 of the Office Action, claims 1-5, 7-13 and 15-19 were rejected under 35 USC 102(e) as anticipated by Lai. The rejections of claims 1 and 9 are moot because said claims are herein canceled and replaced by new claims 21 and 22 respectively. Therefore, claims 21 and 22 will be discussed first, then the rejection of claims 17-20 will be addressed

Claim 21 recites "at least one instruction execution part using the data held by said data holding part to continue execution of said instruction without rerunning said instruction" (claim 20, lines 5-6) which is consistent with the specification at page 10, lines 1-10 and page 16, line 32 to page 17, line 5. What was cited in Lai as allegedly disclosing "re-supplying data lost during an interruption by a target initiated termination request ... [where the] target that initiated the interrupt is not necessarily the target that receives the lost data" (Office Action, page 3, lines 1-3) was "if the PCI (peripheral component interconnect) bus transfer is interrupted, the reload address is supplied to the random access buffer memory to enable data output holding registers to be reloaded with the data lost by the target during the interrupted DMA transfer" (Abstract); "data lost during a PCI burst transfer can be recovered merely by supplying the reload address

data lost by the target during the interrupted DMA transfer" (Abstract); "data lost during a PCI burst transfer can be recovered merely by supplying the reload address to the memory 18a and the address holding register" (column 7, lines 28-30); and "the target interrupts the PCI transfer by deasserting the target ready signal (TRDY#) and asserting the stop signal ... causing the output holding register 92 to hold the data set (D6) on PCI bus 12" (column 12, lines 15-21).

In other words, if a PCI bus transfer is interrupted in the system taught by Lai, the reload address in the reload address register is supplied to the random access buffer memory to enable data output holding registers to be reloaded with the data lost by the target during the interrupted DMA transfer. The reload address register is incremented based on the target successfully receiving a data word. However, reloading and then executing from the beginning, i.e., rerunning, an instruction after an interrupt is not "using the data held by said data holding part to continue execution of said instruction without rerunning said instruction" (claim 21, lines 5-6). Nothing was cited or found in Lai that teaches or suggests the limitation recited on lines 5-6 of claim 21.

Claim 21 also recites "a data holding part holding data of said instruction that is interrupted by said interrupt at a time when said interrupt starts to occur" (claim 21, lines 3-4) which is consistent with the specification at page 9, line 37 to page 10, line 10. What was cited in Lai as allegedly disclosing the data holding part previously recited in claim 1 was "supplying a reload address to a random access memory to resupply data that was lost during interruption of a PCI burst transfer" (column 6, lines 65-67) and "data lost ... can be recovered merely by supplying the reload address to the memory 18a and the address holding register 69" (column 7, lines 28-31). In other words, what was cited in Lai describes after the data is lost, supplying a reload address to memory. Supplying a reload address after data is lost is different than "holding data of said instruction that is interrupted by said interrupt at a time when said interrupt starts to occur" (claim 21, lines 3-4). Nothing was cited or found in Lai that teaches or suggests the limitation recited on lines 3-4 of claim 20.

Furthermore claim 21 recites "an interrupt of a program caused by an exception operation when an instruction is executed" (claim 21, lines 1-2) which is consistent with the specification at page 1, line 14. On the other hand, Lai describes "a DMA transfer on the PCI bus 12" (column 9, lines 60-61), which means a direct memory access data transfer without using a CPU. Thus, an interrupt of a DMA data transfer in Lai cannot be equated with the claimed "interrupt of a program caused by an exception operation" as recited in claim 21. Therefore, for all of the above reasons, claim 21 is allowable.

Claim 22 recites continuing "execution of said instruction without rerunning"; "holding data ... at a time when said interrupt starts to occur" and "exception operation" limitations in a manner similar to claim 21. Dependent claims 2-5, 7 and 8 depend from claim 21; and dependent claims 10-13, 15 and 16 depend from claim 22. Therefore, claims 2-5, 7, 8, 10-13, 15, 16 and 22 distinguish over the applied art for reasons discussed in regard to claim 21.

In rejecting claim 17, column 6, lines 60-67; column 7, lines 12-32 and column 12, lines 16-22 and the Abstract of Lai were cited as disclosing the limitations recited in claim 17. However, as discussed above, if a PCI bus transfer is interrupted in the system taught by Lai, the reload address in the reload address register is supplied to the random access buffer memory to enable data output holding registers to be reloaded with the data lost by the target during the interrupted DMA transfer. Nothing has been cited or found in Lai suggesting "holding in a memory at least an address of an instruction in an operation when interrupt processing that is not caused by the instruction causes the operation to halt; and continuing the operation after the interrupt processing is discontinued" as recited in claim 17.

During the Examiner Interview the Examiner questioned where there was support in the specification for the limitation " interrupt processing that is not caused by the instruction causes the operation to halt" (claim 17, lines 2-3). As described in the specification, "an instruction next to an instruction which has a possibility of being interrupted can be issued without waiting for completion of execution of the instruction which has a possibility of being interrupted" (page 28, lines 8-12). The "instruction" recited in claim 17 corresponds to the first instruction mentioned in the preceding quote. Thus, it is submitted that this limitation is supported by the specification. For the above reasons, it is submitted that claim 17, as well as claims 18-20 which depend therefrom, are allowable.

Furthermore, claim 18 recites "continuing execution of the instruction based on the address held in the memory, after the interrupt processing is discontinued" where the address held in the memory is "an address of an instruction in an operation" (claim 17, line 2) that is held "when interrupt processing ... causes the operation to halt" (claim 17, lines 2-3). As discussed above, Lai discloses rerunning an instruction from the beginning after an interrupt, not continuing execution of the instruction. It is submitted that claim 18, as well as claim 20 which depends therefrom, are allowable for this additional reason.

In addition, claim 20 recites "the interrupt processing is initiated by an exception operation." As discussed above, Lai is directed to a direct memory access data transfer without using a CPU. It is submitted that an interrupt of a DMA data transfer as taught by Lai cannot be

equated with "interrupt processing ... initiated by an exception operation" as recited in claim 20. Therefore, it is submitted that claim 20 is allowable for this additional reason.

Conclusion

It is submitted that Lai does not teach or suggest the features of the present claimed invention. Thus, it is submitted that claims 2-5, 7, 8, 10-13 and 15-22 are in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Finally, if there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: 8/8/06

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Date: August 8, 2006